



09/919495

PTO/SB/21/07-06)

Approved for use through 09/30/2006. OMB 0664-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	Patent#: 7,111,033	
	Filing Date	Issued: September 19, 2006	
	First Named Inventor	Sebastien Ferroussat	
	Art Unit	2193	
	Examiner Name	T. V. Mai	
Total Number of Pages in This Submission	10	Attorney Docket Number	S1022.80718US00

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form  <input type="checkbox"/> Fee Attached  <input type="checkbox"/> Amendment/Reply  <input type="checkbox"/> After Final  <input type="checkbox"/> Affidavits/declaration(s)  <input checked="" type="checkbox"/> Request for Certificate of Correction  <input checked="" type="checkbox"/> Certificate of Correction  <input checked="" type="checkbox"/> Pages 2, 9 & 10 Application as Filed  <input checked="" type="checkbox"/> Columns 1 & 5 of U.S. Patent No. 7,111,033  <input type="checkbox"/> Reply to Missing Parts/Incomplete Application  <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s)  <input type="checkbox"/> Licensing-related Papers  <input type="checkbox"/> Petition  <input type="checkbox"/> Petition to Convert to a Provisional Application  <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address  <input type="checkbox"/> Terminal Disclaimer  <input type="checkbox"/> Request for Refund  <input type="checkbox"/> CD, Number of CD(s) _____  <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC  <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences  <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)  <input type="checkbox"/> Proprietary Information  <input type="checkbox"/> Status Letter  <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below):  Return Receipt Postcard
Remarks		<b>Certificate OCT 16 2006 of Correction</b>

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature			
Printed name	James H. Morris		
Date	October 10, 2006	Reg. No.	34,681

Certificate of Mailing Under 37 CFR 1.8(a)	
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
Dated: October 10, 2006	Signature:  (Gail Driscoll)

OCT 17 2006



Docket No.: S1022.80718US00  
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sebastien Ferroussat  
Serial No.: 09/919,495  
Filed: July 30, 2001  
Patent No.: 7,111,033  
For: CARRY SAVE ADDERS  
Examiner: T. V. Mai  
Art Unit: 2193

Patent No. 7,111,033  
Issued September 19, 2006

Confirmation No.: 4927

Certificate of Mailing Under 37 CFR 1.8(a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: Attention: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: October 10, 2006

  
Gail Driscoll

REQUEST FOR CERTIFICATE OF CORRECTION  
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted typographical errors which should be corrected.

In the Specification:

In column 1, line 51, of U.S. Patent No. 7,111,033 the text currently reads:

of one sum **bet** and two carry bits. One of these carry bits is (Emphasis added).

The corresponding text found on page 2, line 2 of the application as filed is reproduced below.

of one sum **bit** and two carry bits. One of these carry bits is (Emphasis added).

In column 5, line 12, of U.S. Patent No. 7,111,033 the text currently reads:

**circumstance** the value zero would be taken as the input to (Emphasis added).

OCT 17 2006

The corresponding text found on page 9, line 11 of the application as filed is reproduced below.

**circumstances** the value zero would be taken as the input to (Emphasis added).

In column 5, line 53, of U.S. Patent No. 7,111,033 the text currently reads:

Reference **in** now made to FIG. 6 which shows a 7 to 4 (Emphasis added).

The corresponding text found on page 10, line 18 of the application as filed is reproduced below.

Reference **is** now made to FIG. 6 which shows a 7 to 4 (Emphasis added).

No amendments were made by either the Examiner or Patentee to change the word "bit" to "bet", "circumstance" to "circumstances" or to change "is" to "in".

In support of this request, Patentee enclosed highlighted copies of pages 2, 9 and 10 of the application as filed and columns 1 and 5 of U.S. Patent No. 7,111,033.

Patentee respectfully submits that, since the errors for which a Certificate of Correction is sought were the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: October 10, 2006

Respectfully submitted,

By: 

James H. Morris

Registration No.: 34,681

WOLF, GREENFIELD & SACKS, P.C.

Federal Reserve Plaza

600 Atlantic Avenue

Boston, Massachusetts 02210-2206

(617) 646-8000

OCT 17 2006

1

**CARRY SAVE ADDERS****FIELD OF THE INVENTION**

The present invention relates to carry save adders and in particular but not exclusively to carry save adders which are able to reduce the number of partial products to two.

**BACKGROUND TO THE INVENTION**

In digital arithmetic, partial products are obtained when two numbers are multiplied together. The number of partial products will depend on the method used for obtaining the partial products. In a conventional operation, the number of partial products may be equal to the number of bits in the multiplier. However, techniques such as Booth encoding make it possible to reduce the number of partial products obtained. For example Booth coding allows the number of partial products to be reduced by a factor of 2. The Booth encoding method is sometimes referred to as the Booth-MacSorley algorithm.

In the Booth coding method, a triplet of bits of the multiplier is input to a Booth coder which provides three outputs, the values of which depends on the input values. The outputs of the Booth coder are then used to modify bits of the number to be multiplied by the multiplier.

Carry save adders which reduce three partial products to two partial products are known. This type of carry save adder is sometimes referred to as a 3 to 2 carry save adder. Such a carry save adder is in fact a full adder. A full adder is a binary logic circuit which produces a two-bit sum where one bit represents the sum and the other bit represents the carry when three one bit binary numbers are added together. The three one bit numbers may be corresponding bits from three partial products.

Carry save adders which reduce four partial products to two partial products are also known. This type of carry save adder is known as a 4 to 2 carry save adder. One example of such a carry save adder is shown in the IEEE Journal of Solid State circuits, Vol 30, No 3, March 1995: "A 4.4 ns CMOS 54x54-b using pass-transistor multiplexer", page 251 to 257, N Ohkubo et al. This structure generally yields faster partial product compression than the use of 3 to 2 carry save adders. The 4 to 2 carry save adder actually compresses five partial products into three and is therefore sometimes referred to as a 5 to 3 carry save adder. This carry save adder is connected in such a way that four of the inputs are corresponding bits from four partial products whilst the fifth input is fed from a neighbouring adder and is known as the "carry in". The output of this carry save adder consists of one sum bit and two carry bits. One of these carry bits is input to a neighbouring carry save adder and forms one of the five inputs of that carry save adder.

**SUMMARY OF THE INVENTION**

It is an aim of embodiments of the present invention to provide a carry save adder unit which is capable of compressing more than five inputs to a smaller number of outputs.

According to one aspect of the present invention, there is provided a carry save adder for reducing the number of inputs to a lower number of outputs, said carry save adder comprising four carry save adders, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a

2

second of said layers, said third and fourth carry save adders being arranged to provide said outputs, said third and fourth carry save adders each receiving at least one output from each of said first and second carry save adders and the first and second carry save adders being arranged to receive at least some of said inputs.

This arrangement permits a relatively short routing between the carry save adders to be achieved. This may also improve timing.

At least one of the inputs may be input to at least one of the third and fourth carry save adders.

The carry save adder circuit may be a 9 to 4 carry save adder circuit. The first carry save adder may be a 5 to 3 carry save adder and the second, third and fourth carry save adders may be 3 to 2 carry save adders. The first to fifth inputs may be input to the first carry save adder and the sixth to eighth inputs may be provided to the second carry save adder. The ninth input may be input directly to one of the third and fourth carry save adders.

The carry save adder circuit may alternatively be a 7 to 4 carry save adder circuit. The first to third carry save adders may be 3 to 2 carry save adders and the fourth carry save adder may be a half adder. The first to third inputs may be input to the first carry save adder and the fourth to sixth inputs may be provided to the second carry save adder. The seventh input may be input directly to one of the third and fourth carry save adders.

According to a second aspect of the present invention there is provided a carry save adder circuit for reducing nine inputs to four outputs, said carry save adder circuit comprising four carry save adders, the first carry save adder being a 5 to 3 carry save unit and the second, third and fourth carry save adders being 3 to 2 carry save adders.

According to a third aspect of the present invention there is provided a carry save adder circuit for reducing seven inputs to four outputs, said carry save adder circuit comprising four carry save adders, the first, second and third carry save adders being 3 to 2 carry save adders and the fourth carry save unit being a half adder.

According to a fourth aspect of the present invention there may be provided an arithmetic unit for processing a plurality of partial products, said unit comprising a plurality of carry save adder circuits as claimed in any preceding claim, wherein the inputs to each of said carry save adder circuits are provided by said plurality of partial products.

**BRIEF DESCRIPTION OF THE DRAWINGS**

For a better understanding of the present invention and as to how the same may be carried into effect, reference will now be made by way of example to the accompanying drawings in which:

FIG. 1 shows a 3 to 2 carry save adder;

FIG. 2 shows a 5 to 3 carry save adder;

FIG. 3 shows three 5 to 3 carry save adders connected together in series and used as 4 to 2 carry save adders;

FIG. 4 shows a 9 to 4 carry save adder embodying the present invention;

FIG. 5 shows an arithmetic unit embodying the present invention;

FIG. 6 shows a 7 to 4 carry save adder embodying the present invention;

FIG. 7 shows one possible structure of a 3 to 2 carry save adder;

FIG. 8 shows one possible structure of a 5 to 3 carry save adder; and

5

Each partial product P0 to P8 has n bits. One bit from each of the partial products is input to the carry save adder 20 of FIG. 4. If the mth bit of the first partial product P0 is selected, the  $m-2^{\text{th}}$  bit will be selected from the second partial product P1, the  $m-4^{\text{th}}$  bit selected from the third partial product P2 and so on. In this scenario, the first bit in a given partial product is the least significant bit whilst the nth bit in the partial product is the most significant bit. In certain cases, there will be no bits available. For example, if  $m=4$ , the corresponding bit from the fourth partial product P3 would be  $m=2$ . This gives a negative value. In these circumstances the value zero would be taken as the input to the carry save adder. Effectively the values of the partial products are offset so as to take into account the significance or weight of each of the partial product.

The number of carry save adders 20 which are provided is defined by the following equation:

$$\text{number of bits} = n + 2(p-1) \text{ where}$$

n is the number of bits in each partial products

p is the number of partial products.

As discussed above, there are not always 9 bits. For example column 5 only has three bits. In those circumstances it is not necessary to use the 9 to 4 adder. Instead, a 3 to 2 carry save adder can be used. Accordingly, the carry save adder for each column can be selected in accordance with the number of bits which are to be added.

Each carry save adder provides four outputs as discussed in relation to FIG. 4. The sum output S of the third carry save adder 26 provides one bit of a first partial product 34, the second output C02A of the third carry save adder 26 provides one bit of a second partial product 36, the first output C02B of the fourth carry save adder 28 provides one bit of the third partial product 38 and the second output C04 of the fourth carry save adder 28 provides one bit of a fourth partial product 40. The first output of the carry save adder 20 provides the mth position of the first partial product 34. The second and third outputs C02A and C02B provide the  $m+1$ th positions of the second and third partial products 36 and 38. The fourth output of the carry save adder C04 provides the  $m+2$ th position of the fourth partial product 40. The positions to which the outputs of the carry save adder 20 are provided in the respective partial products 34 to 40 reflects their significance or weight. The outputs of adjacent carry save adders are at adjacent locations in the partial products 34 to 40.

These four partial products 34 to 40 which receive the outputs of the carry save adder 20 are input to respective 4 to 2 adders which reduce the number of partial products to two. These two partial products can then be summed to provide a single result.

Reference is now made to FIG. 6 which shows a 7 to 4 carry save adder 50. The 7 to 4 carry save adder 50 comprises four carry save adders 52 to 58. The first, second and third carry save adders 52 to 56 are 3 to 2 adders, such as illustrated in FIG. 1. The fourth carry save adder 58 is a half adder which receives two inputs and provides two outputs.

The first carry save adder 52 receives the first to third inputs 11, 12 and 13. The second carry save adder 54 receives the fourth fifth and sixth inputs 14, 15 and 16. The sum output S of the first carry save adder 52 provides the first input a to the third carry save adder 56. The sum output of the second carry save adder 54 provides the second input b to the third carry save adder 56. The third input to the third carry save adder 56 is provided by the seventh input 17.

6

The fourth carry save adder 58 receives the carry output C01 of the first and the second carry save adders which provide the first and second inputs a and b respectively.

The output of the third carry save adder provides the output S as its sum output and the output C02A as its carry output. The sum output of the fourth carry save adder 58 provides the second carry output C02B output whilst the carry output of the fourth carry save adder 58 provides the carry output C04. These outputs have the same significance or weight as those outputs of the 9 to 4 carry save adder shown in FIG. 4.

The seventh input 17 is faster than the other inputs in that it only has to pass through one of the carry save adders. The first and second carry save adders 52 and 54 receive the first six inputs 11 to 16. The first and second carry save adders 52 and 54 effectively provide a first layer. The third carry save adder 56 and the half adder 58 provide a second layer and receive the respective outputs from the first layer as well as the seventh input 17. In practice, the adders making up the carry save adder of FIG. 6 can be arranged in any suitable way so as to minimise the length of the connections as with the embodiment described in relation to FIG. 4.

The carry save adder of FIG. 6 can also be used in a similar context to that shown in FIG. 5 if seven partial products are generated, particularly if seven bits are to be processed in a column. The carry save adder can also be used in the embodiment shown in FIG. 5 where there are more than seven partial products but only seven bits are provided for a given column.

It should be noted that, as with the carry save adder of FIG. 4, some of the interconnections between the carry save adders making up the 7 to 4 carry save adder can be altered without altering the function of the adder as a whole. For example the inputs to the third carry save adder 56 can be swapped with other inputs to that carry save adder. Likewise the inputs to the half adder 58 can be swapped around.

Again a 4 to 2 carry save adder can be provided to reduce the number of partial products to two.

The arrangement of both the 9 to 4 and the 7 to 4 carry save adders allow short routings to be achieved between the carry save adders. This improves both timing and routing of these carry save adders. This is particularly advantageous when embodiments of the present invention are incorporated in an integrated circuit.

Reference is made to FIG. 3 which shows three of the carry save adders 6a, 6b and 6c of FIG. 2 connected together. Each of the 5 to 3 carry save adders 6 receives inputs A to D and the input CI from the preceding carry save adder and provides three outputs as in FIG. 2. The first carry save adder block 6a receives a carry input CI from a preceding carry save adder. If there is no previous carry save adder, then input CI will be zero. The first carry save adder 6a outputs the second carry output C02 to the second carry save adder 6b. This second carry output C02 from the first carry save adder is the carry input CI to the second carry save adder 6b. Likewise, the second carry save adder 6b provides its second carry output C02 as the carry input CI to the third carry save adder 6c. It should be noted that the input CI is not used to generate the C02 output of the same carry save adder.

This means that the carry propagation is only done from one carry save adder to the next. The respective inputs A to D to each of the carry save adders 6 may represent adjacent bits from four partial products. For example, the first carry save adder 6a receives the nth bit of first, second, third and fourth partial products with the second and third carry save adders 6b and 6c receiving the  $n+1$  and  $n+2$  bits respectively of those same partial products.

three one bit binary numbers are added together. The three one ~~bit~~ numbers may be corresponding bits from three partial products.

Carry save adders which reduce four partial products to two partial products are also known. This type of carry save adder is known as a 4 to 2 carry save adder. One example of such a carry save adder is shown in the IEEE Journal of Solid State circuits, Vol 30, No 3, March 1995: "A 4.4ns CMOS 54x54-b using pass-transistor multiplexer", page 251 to 257, N Ohkubo et al. This structure generally yields faster partial product compression than the use of 3 to 2 carry save adders. The 4 to 2 carry save adder actually compresses five partial products into three and is therefore sometimes referred to as a 5 to 3 carry save adder. This carry save adder is connected in such a way that four of the inputs are corresponding bits from four partial products whilst the fifth input is fed from a neighbouring adder and is known as the "carry in". The output of this carry save adder consists of one sum bit and two carry bits. One of these carry bits is input to a neighbouring carry save adder and forms one of the five inputs of that carry save adder.

#### Summary of the Invention

It is an aim of embodiments of the present invention to provide a carry save adder unit which is capable of compressing more than five inputs to a smaller number of outputs.

According to one aspect of the present invention, there is provided a carry save adder for reducing the number of inputs to a lower number of outputs, said carry save adder comprising four carry save adders, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a second of said layers, said third

Each partial product P0 to P8 has n bits. One bit from each of the partial products is input to the carry save adder 20 of Figure 4. If the mth bit of the first partial product P0 is selected, the m-2<sup>th</sup> bit will be selected from the second partial product P1, the m-4<sup>th</sup> bit selected from the third partial product P2 and so on. In this scenario, the first bit in a given partial product is the least significant bit whilst the nth bit in the partial product is the most significant bit. In certain cases, there will be no bits available. For example, if m=4, the corresponding bit from the fourth partial product P3 would be m=-2. This gives a negative value. In these circumstances the value zero would be taken as the input to the carry save adder. Effectively the values of the partial products are offset so as to take into account the significance or weight of each of the partial product.

The number of carry save adders 20 which are provided is defined by the following equation:

number of bits =  $n + 2(p-1)$  where

n is the number of bits in each partial products

p is the number of partial products.

As discussed above, there are not always 9 bits. For example column 5 only has three bits. In those circumstances it is not necessary to use the 9 to 4 adder. Instead, a 3 to 2 carry save adder can be used. Accordingly, the carry save adder for each column can be selected in accordance with the number of bits which are to be added.

Each carry save adder provides four outputs as discussed in relation to Figure 4. The sum output S of the third carry save adder 26 provides one bit of a first partial product 34, the second output C02A of the third carry save adder 26 provides one bit of a second partial product 36, the first output C02B of the

fourth carry save adder 28 provides one bit of the third partial product 38 and the second output C04 of the fourth carry save adder 28 provides one bit of a fourth partial product 40. The first output of the carry save adder 20 provides the mth position of the first partial product 34. The second and third outputs C02A and C02B provide the m+1th positions of the second and third partial products 36 and 38. The fourth output of the carry save adder C04 provides the m+2th position of the fourth partial product 40. The positions to which the outputs of the carry save adder 20 are provided in the respective partial products 34 to 40 reflects their significance or weight. The outputs of adjacent carry save adders are at adjacent locations in the partial products 34 to 40.

These four partial products 34 to 40 which receive the outputs of the carry save adder 20 are input to respective 4 to 2 adders which reduce the number of partial products to two. These two partial products can then be summed to provide a single result.

Reference is now made to Figure 6 which shows a 7 to 4 carry save adder 50. The 7 to 4 carry save adder 50 comprises four carry save adders 52 to 58. The first, second and third carry save adders 52 to 56 are 3 to 2 adders, such as illustrated in Figure 1. The fourth carry save adder 58 is a half adder which receives two inputs and provides two outputs.

The first carry save adder 52 receives the first to third inputs 11, 12 and 13. The second carry save adder 54 receives the fourth fifth and sixth inputs 14, 15 and 16. The sum output S of the first carry save adder 52 provides the first input a to the third carry save adder 56. The sum output of the second carry save adder 54 provides the second input b to the third carry save adder 56. The third input to the third carry save adder 56 is provided by the seventh input 17.



**UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION**

Page 1 of 1

PATENT NO. : 7,111,033  
APPLICATION NO. : 09/919,495  
ISSUE DATE : September 19, 2006  
INVENTOR(S) : Sebastien Ferroussat

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, line 51 should read:  
of one sum bit and two carry bits. One of these carry bits is

Column 5, line 12 should read:  
circumstances the value zero would be taken as the input to  
line 53 should read:  
Reference is now made to FIG. 6 which shows a 7 to 4

MAILING ADDRESS OF SENDER (Please do not use customer number below):

James H. Morris  
WOLF, GREENFIELD & SACKS, P.C.  
Federal Reserve Plaza  
600 Atlantic Avenue  
Boston, Massachusetts 02210-2206

**OCT 17 2006**